AMENDMENT TO THE CLAIMS

1. (currently amended) A method of making an electrically programmable memory element, comprising:

providing a first dielectric layer, said first dielectric layer having an opening, said opening having a sidewall surface and a bottom surface;

forming a conductive ~~sidewall spacer~~ layer ~~over~~ on said sidewall surface and said bottom surface;

removing at least a portion of said conductive layer from said bottom surface;

forming a second dielectric layer on said conductive ~~sidewall spacer~~ layer within said opening; and

forming a programmable resistance material in ~~electrical contact with a top surface of said conductive sidewall spacer~~ electrical communication with said conductive layer.

Claims 2-6 (canceled)

7. (original) The method of claim 1, wherein said programmable resistance material is a phase-change material.

8. (original) The method of claim 1, wherein said programmable resistance material includes a chalcogen element.

9. (original) The method of claim 1, wherein said first dielectric layer and said second dielectric layer are formed of the same material.

Claims 10-15 (Cancelled)

16. (new) The method of claim 1, wherein said forming said conductive layer step comprises substantially conformally depositing said conductive layer on said sidewall surface and said bottom surface.

17. (new) The method of claim 1, wherein said removing step comprises substantially anisotropically etching said conductive layer.

18. (new) The method of claim 1, wherein said programmable resistance material is electrically coupled to a top surface of said conductive layer.

19. (new) The method of claim 1, wherein after said removing step, said conductive layer includes a conductive sidewall spacer.

20. (new) A method of making an electrically programmable memory element, comprising:

providing a sidewall surface and an adjoining bottom surface;

forming a conductive layer on said sidewall surface and said bottom surface;

removing at least a portion of said conductive layer from said bottom surface; and

forming a programmable resistance material in electrical communication with said conductive layer.

21. (new) The method of claim 20, wherein said forming said conductive layer step comprises substantially conformally depositing said conductive layer on said sidewall surface and said bottom surface.

22. (new) The method of claim 20, wherein said removing step comprises substantially anisotropically etching said conductive layer.

23. (new) The method of claim 20, wherein said programmable resistance material is electrically coupled to a top surface of said conductive layer.

24. (new) The method of claim 20, further comprising forming a dielectric layer on said conductive layer after said removing step.

25. (new) The method of claim 24, wherein said dielectric layer is formed on said conductive layer before said forming said programmable resistance material step.

26. (new) The method of claim 20, wherein said sidewall surface is the sidewall surface of a first dielectric layer.

27. (new) The method of claim 26, further comprising forming a second dielectric layer on said conductive layer after said removing step.

28. (new) The method of claim 27, wherein said second dielectric layer is formed before said forming said programmable resistance material step.

29. (new) The method of claim 27, wherein said first dielectric layer and said second dielectric layer are formed of the same material.

30. (new) A method of making an electrical device, comprising:

providing a sidewall surface and an adjoining bottom surface;

forming a conductive layer on said sidewall surface and said bottom surface;

removing at least a portion of said conductive layer from said bottom surface; and

forming a chalcogenide material in electrical communication with said conductive layer.

31. (new) The method of claim 30, wherein said forming said conductive layer step comprises substantially conformally depositing said conductive layer on said sidewall surface and said bottom surface.

32. (new) The method of claim 30, wherein said removing step comprises substantially anisotropically etching said conductive layer.

33. (new) The method of claim 30, wherein said programmable resistance material is electrically coupled to a top surface of said conductive layer.

34. (new) The method of claim 30, further comprising forming a dielectric layer on said conductive layer after said removing step.

35. (new) The method of claim 34, wherein said dielectric layer is formed before said forming said programmable resistance material step.

36. (new) The method of claim 30, wherein said sidewall surface is the sidewall surface of a first dielectric layer.

37. (new) The method of claim 36, further comprising forming a second dielectric layer on said conductive layer after said removing step.

38. (new) The method of claim 37, wherein said second dielectric layer is formed before said forming said programmable resistance material step.

39. (new) The method of claim 37, wherein said first dielectric layer and said second dielectric layer are formed of the same material.

40. (new) The method of claim 30, wherein after said removing step, said conductive layer includes a conductive sidewall spacer.

41. (new) A method of making an electrical device, comprising:

forming an electrical contact by a method comprising

providing a sidewall surface and an adjoining bottom surface,

forming a conductive layer on said sidewall surface and said bottom surface,

removing at least a portion of said conductive layer from said bottom surface; and

forming a chalcogenide material, said chalcogenide material in electrical communication with said electrical contact.

42. (new) The method of claim 41, wherein said forming said conductive layer step comprises substantially conformally depositing said conductive layer on said sidewall surface and said bottom surface.

43. (new) The method of claim 41, wherein said removing step comprises substantially anisotropically etching said conductive layer.

44. (new) The method of claim 41, wherein said chalcogenide material is formed after forming said electrical contact.

45. (new) The method of claim 41, wherein said electrical contact is a conductive sidewall spacer.

46. (new) The method of claim 41, wherein said sidewall surface is the sidewall surface of a dielectric layer.

47. (new) A method of making an electrical device, comprising:

forming an electrical contact by a method comprising

providing a sidewall surface and an adjoining bottom surface,

forming a conductive layer on said sidewall surface and said bottom surface,

removing at least a portion of said conductive layer from said bottom surface; and

forming a phase-change material,

said phase-change material in electrical communication with said electrical contact.

48. (new) The method of claim 47, wherein said forming said conductive layer step comprises substantially conformally depositing said conductive layer on said sidewall surface and said bottom surface.

49. (new) The method of claim 47, wherein said removing step comprises substantially anisotropically etching said conductive layer.

50. (new) The method of claim 47, wherein said phase-change material is formed after forming said electrical contact.

51. (new) The method of claim 47, wherein said electrical contact is a conductive sidewall spacer.

52. (new) The method of claim 47, wherein said sidewall surface is the sidewall surface of a dielectric material.

53. (new) The method of claim 47, wherein said phase-change material comprises at least one chalcogen element.